DATA PROCESSING APPARATUS WITH REGISTER FILE BYPASS

ABSTRACT OF THE DISCLOSURE

Sub A1

A data processing apparatus for increasing the speed of data transfer from one processor instruction to another processor instruction. First (**78**) and second (**80**) functional unit groups, each including a plurality of functional units, are connected to a register file (**76**) comprising a plurality of registers having corresponding register numbers. A comparator (**181**) receives an indication of the operand register number of a current instruction for a functional unit in the first functional unit group, and an indication of the destination register number of an immediately preceding instruction for the second functional unit group, and indicates whether the register numbers match. A register file bypass multiplexer (**174**) has a first input receiving data from the register corresponding to the operand register number of the current instruction, a second input (hotpath **172**) connected to the output of the second functional unit group, and an output supplying an operand to the operand input of the first functional unit group. The multiplexer selects the data from the register corresponding to the operand number of the current instruction if the first comparator fails to indicate a match and selects the output of the second functional unit group if the comparator indicates a match. The first functional unit utilizes the output of the second functional unit group without waiting for the result to be stored in the register file, thus avoiding excess delay slots in the instruction pipeline.